What Is Claimed Is:

1. A method for speeding up processing of a layout of an integrated circuit that has been divided into cells the method comprising:

determining if a target cell in the layout is identical to a preceding cell for which there exists a previously calculated solution by comparing a hash code created from the target cell with a hash code created from the preceding cell;

if the target cell is identical to the preceding cell, using the previously calculated solution as a solution for the target cell; and

otherwise, if the target cell is not identical to the preceding cell, processing the target cell to produce the solution for the target cell.

2. The method of claim 1, wherein if the hash code created from the target cell matches the hash code created from the preceding cell, the method further comprises comparing the complete layout of the target cell with the complete layout of the preceding cell to ensure that the target cell is identical to the preceding cell.

3. The method of claim 1, wherein determining if the target cell is identical to a preceding cell involves determining whether an area surrounding the target cell is identical to an area surrounding the preceding cell.

4. The method of claim 1, wherein prior to determining if the target cell is identical to the preceding cell, the method further comprises performing an overlap removal operation on the target cell and the preceding cell.

5. The method of claim 1, wherein prior to considering the target cell, the method further comprises:

receiving a specification for the layout of the integrated circuit; and

dividing the layout into a plurality of cells, whereby each cell can be independently processed.

6. The method of claim 5, further comprising distributing the plurality of cells to a set of parallel processors so that plurality of cells can be processed in parallel.

7. The method of claim 1, wherein processing the target cell involves performing one of:

model-based optical proximity correction (OPC);

rule-based optical proximity correction; and

phase shifter assignment for the target cell.

8. A computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method for speeding up processing of a layout of an integrated circuit that has been divided into cells, the method comprising:

determining if a target cell in the layout is identical to a preceding cell for which there exists a previously calculated solution by comparing a hash code created from the target cell with a hash code created from the preceding cell;

if the target cell is identical to the preceding cell, using the previously calculated solution as a solution for the target cell; and

otherwise, if the target cell is not identical to the preceding cell, processing the target cell to produce the solution for the target cell.

9. The computer-readable storage medium of claim 8, wherein if the hash code created from the target cell matches the hash code created from the preceding cell, the method further comprises comparing the complete layout of the target cell with the complete layout of the preceding cell to ensure that the target cell is identical to the preceding cell.

10. The computer-readable storage medium of claim 8, wherein determining if the target cell is identical to a preceding cell involves determining whether an area surrounding the target cell is identical to an area surrounding the preceding cell.

11. The computer-readable storage medium of claim 8, wherein prior to determining if the target cell is identical to the preceding cell, the method further comprises performing an overlap removal operation on the target cell and the preceding cell.

12. The computer-readable storage medium of claim 8, wherein prior to considering the target cell, the method further comprises:

receiving a specification for the layout of the integrated circuit; and

dividing the layout into a plurality of cells, whereby each cell can be independently processed.

13. The computer-readable storage medium of claim 12, wherein the method further comprises distributing the plurality of cells to a set of parallel processors so that plurality of cells can be processed in parallel.

14. The computer-readable storage medium of claim 8, wherein processing the target cell involves performing one of:

model-based optical proximity correction (OPC);

rule-based optical proximity correction; and

phase shifter assignment for the target cell.

15. An apparatus for speeding up processing of a layout of an integrated circuit that has been divided into cells, the apparatus comprising:

a comparison mechanism that is configured to determine if a target cell in the layout is identical to a preceding cell for which there exists a previously calculated solution by comparing a hash code created from the target cell with a hash code created from the preceding cell;

a processing mechanism that is configured to produce a solution for the target cell;

wherein if the target cell is identical to the preceding cell, the target cell is configured to use the previously calculated solution as the solution for the target cell; and

wherein if the target cell is not identical to the preceding cell, the processing mechanism is configured to process the target cell to produce the solution for the target cell.

16. The apparatus of claim 15, wherein if the hash code created from the target cell matches the hash code created from the preceding cell, the comparison mechanism is configured to compare the complete layout of the target cell with the complete layout of the preceding cell to ensure that the target cell is identical to the preceding cell.

17. The apparatus of claim 15, wherein the comparison mechanism is configured to determine whether an area surrounding the target cell is identical to an area surrounding the preceding cell.

18. The apparatus of claim 15, further comprising an overlap removal mechanism that is configured perform an overlap removal operation on the target cell and the preceding cell before the comparison mechanism compares the target cell with the preceding cell.

19. The apparatus of claim 15, further comprising a partitioning mechanism that is configured to:

receive a specification for the layout of the integrated circuit; and to

divide the layout into a plurality of cells, whereby each cell can be independently processed.

20. The apparatus of claim 19, further comprising a distribution mechanism that is configured to distribute the plurality of cells to a set of parallel processors so that plurality of cells can be processed in parallel.

21. The apparatus of claim 19, wherein the processing mechanism is configured to perform one of:

model-based optical proximity correction (OPC);

rule-based optical proximity correction; and

phase shifter assignment for the target cell.

22. A mask to be used in an optical lithography process, wherein the mask is created through a method that speeds up processing of a layout of an integrated circuit that has been divided into cells, the method comprising:

determining if a target cell in the layout is identical to a preceding cell for which there exists a previously calculated solution;

if the target cell is identical to the preceding cell, using the previously calculated solution as a solution for the target cell; and

otherwise, if the target cell is not identical to the preceding cell, processing the target cell to produce the solution for the target cell.

23. An integrated circuit created through a method that speeds up processing of a layout of an integrated circuit that has been divided into cells, the method comprising:

determining if a target cell in the layout is identical to a preceding cell for which there exists a previously calculated solution;

if the target cell is identical to the preceding cell, using the previously calculated solution as a solution for the target cell; and

otherwise, if the target cell is not identical to the preceding cell, processing the target cell to produce the solution for the target cell.

24. A method for performing distributed mask data preparation and model-based optical proximity correction, comprising:

dividing an input layout into a plurality of jobs, wherein each job involves performing model-based optical proximity correction on a different portion of the layout;

distributing the plurality of jobs across a plurality of processors; and

performing model-based optical proximity correction on the plurality of jobs in parallel on the plurality of processors.

25. The method of claim 24, further comprising:

determining if a portion of the layout associated with a first job is identical to a portion of a layout associated with a second job for which there exists a previously calculated solution by comparing a hash code created from the portion of the layout associated with the first job with a hash code created from the portion of the layout associated with the second job;

if the determination indicates the respective portions of the layout are identical, using the previously calculated solution for the second job as a solution for the first job; and

otherwise, performing model-based optical proximity correction on the portion of the layout associated with the first job to produce the solution for the first job.

26. The method of claim 25, wherein if the hash code created for the first job matches the hash code created for the second job, the method further comprises comparing the portion of the layout associated with the first job with the portion of the layout associated with the second job to ensure that the respective portions of the layout are identical.

27. The method of claim 25, wherein prior to determining if the layout portions are identical, the method further comprises performing an overlap removal operation on the portion of the layout associated with the first job and the portion of the layout associated with the second job.